IN THE SPECIFICATION

Please amend paragraph [0030] of the specification as indicated below:

[0030] In addition, the structure of the functional blocks shown in **Fig. 3** are such that the calibration process does not place the actual termination or reference levels used in the I/O buffer 312 within the "control loop" that is formed between the calibration circuit 308 and the controller 304. This loop is formed by the controller providing the calibration circuit with enable signals compen and txcompen which are used to configure the calibration circuit 308 for the calibration process of each of the three states mentioned above. The controller 304 provides the calibration circuit 308 with changing binary numbers compout [23:0] (to set the digitally-controllable reference signal level), rxcompout [19:0] (to set the digitally-controllable transmission line termination used for calibrating the receiver circuit 320), and txcompout [19:0] (to set the digitally-controllable transmission line termination that is used to calibrate the driver circuit 330). Calibrated values for these variables are determined by the controller 304 in response to the countup, rxcountup, and txcountup signals being asserted (or exhibiting a certain pattern) by the calibration circuit 308. The updates to the actual terminations and reference levels used in the driver circuit 330 and receiver circuit 320 are made, in this embodiment, by the controller 302 providing a separate pair of binary values rxtermout and txtermout to the calibration circuit 308, which in turn provides the actual values for setting the digitally variable termination and reference levels in the I/O buffer 312. The difference between rxtermout and rxcompout, for example, may be an offset value that has been combined with rxcompout (by the controller 304). The offset value may be stored in a configuration register ~~316~~ 314 and set via a host or user programmable interface (*e.g.*, under control of a platform management unit of a computer system). The use of an offset value makes the design applicable to a wider range of impedance matching (*e.g.*, a greater range of termination resistance values or signal reference values).

Please amend paragraph [0032] of the specification as indicated below:

[0032] The configuration registers ~~316~~ 314 may be used to store override compensation values that may be used in, for example, special test modes of operation. In that case, the IC device, instead of applying the calibrated compensation values, applies one or more of the override compensation values (in response to their respective enable signals txcompovren, rxcompovren, and compovren being asserted), to set any one of the reference level, driver termination, and receiver termination of the I/O buffer 312.

Please amend paragraph [0035] of the specification as indicated below:

[0035] The output of the counter 404 may be combined with an offset value (provided from a configuration register ~~316~~ 314, **Fig. 3**). This adjusted value is then used as the selection input to a lookup table or multiplexor 416. In this example, the select input to the multiplexor 416 is an 8-bit value, which is decoded into a 24-bit value. If the compensation override signal is not asserted, then this 24-bit value is forwarded as the compout [23:0] that will be used to actually set the variable termination or reference level in the calibration circuit 308. The same circuit illustrated in **Fig. 4** may be used to generate all the binary values for all three calibration operations, including driver termination, receiver termination, and I/O buffer reference level.

Please amend paragraph [0036] of the specification as indicated below:

[0036] In **Fig. 5**, an example schematic of the calibration circuit 308 is shown. This particular implementation uses a complementary metal oxide semiconductor (CMOS) fabrication process, although other integrated circuit fabrication processes may alternatively be used. The multi-bit binary values (provided by the controller 304) are indicated by the thick lines, whereas the analog signals are present on the thin lines. Beginning with the I/O buffer reference level, this reference level is, in this example, a current that is set by the binary value fed to the variable resistance 404 which is part of the circuit that includes transistors M1-M3. The signal that is actually calibrated, by the

process of adjusting the variable resistance 404, is in this embodiment, a voltage at node 420. The voltage at node 420 also happens to be the signal that will be calibrated for the receiver termination process. In the latter process, the binary value rxcompout is used to set the variable resistance 412 to calibrate the voltage at node ~~20~~ 420. As to the driver termination, that aspect is calibrated by controlling the variable resistance 408, to calibrate the voltage at node 430.

Please amend paragraph [0047] of the specification as indicated below:

[0047] Note also that the calibration circuit 308 and the state machine controller 304 may be stand alone functional blocks that do not rely upon the core logic of the IC device to be running. Rather, a clock signal and the power supply voltage may be all that is needed to launch the controller 304 and calibration circuit 308 into the calibration process described above. Indeed, the provision of the offset values or the override values from the configuration registers ~~316~~ 314 are optional in that they do not need to be implemented in all embodiments of **Fig. 3**.